IN THE CLAIMS:

Please revise the claims to read as follows:

1. (Currently amended) A ring oscillator comprising an odd number of elements interconnected in a serially-connected infinite loop, each said element having an associated ~~programmable~~ delay unit, each said delay unit having a programmable delay.

2. (Original claim) The ring oscillator of claim 1, further comprising:

an input to receive an input signal to start an oscillation of said ring oscillator.

3. (Original claim) The ring oscillator of claim 1, further comprising:

an input to receive an input signal to program each said programmable delay.

4. (Original claim) The ring oscillator of claim 1, wherein each said element comprises a non-inverting amplifier.

5. (Original claim) The ring oscillator of claim 1, wherein said input for said programmable delay provides an adjustment of a duty factor of an output signal of said ring oscillator.

6. (Original claim) The ring oscillator of claim 1, wherein each said element comprises at least one complementary metal oxide semiconductor (CMOS) inverter.

7. (Original claim) The ring oscillator of claim 3, wherein said programmable delay comprises a binary word serving as a vector input.

8. (Original claim) A circuit for testing effects of Negative Bias Temperature Instability (NBTI) on an integrated circuit, said circuit comprising:

a ring oscillator according to claim 1.

9. (Currently amended) A test circuit to measure a Negative Bias Temperature Instability (NBTI) effect for PFETs (p-channel MOSFET) by stressing a target PFET component with at least one stress condition, said target PFET component being integrated as a component into said test circuit, said target PFET component having a source, a drain, and a gate, said test circuit comprising:

a ring oscillator comprising an odd number of oscillator elements interconnected serially in an infinite loop, wherein at least one said target PFET component is integrated into said ring oscillator, said target PFET being integrated into said ring oscillator in such configuration that hot carrier effects from other components in said test circuit do not affect said NBTI effect; and

a test output providing a point to measure at least one parameter of said ring oscillator.

10. (Original claim) The NBTI test circuit of claim 9, wherein each said oscillator element contains at least one said target PFET.

11. (Original claim) The NBTI test circuit of claim 9, further comprising:

a switching circuit to selectively switch said at least one stress condition onto said target PFET.

12. (Original claim) The NBTI test circuit of claim 11, wherein said at least one stress condition comprises at least one of:

a DC stress, wherein said target PFET receives a first constant voltage level on said gate and a second constant voltage level on said source and drain;

an AC stress, wherein said target PFET receives a varying voltage on said gate; and

a free running mode, wherein said target PFET receives a varying complementary voltage on said drain and said gate.

13. (Original claim) The NBTI test circuit of claim 11, wherein said target PFET is stressed by an AC stress by selectively applying a gate pulse, said gate pulse being adjustable in at least one of frequency and duty factor.

14. (Currently amended) A method of testing a PFET (p-channel field effect transistor), comprising:

incorporating a target PFET into a ring oscillator having an odd number of elements;

performing at least one stress test on said PFET; and

measuring at least one characteristic of said ring oscillator <u>based on independently controlling both a frequency parameter and a duty factor parameter of said ring oscillator</u>.

15. (Original claim) The method of claim 14, wherein said each said ring oscillator element contains a variable delay.

16. (Original claim) The method of claim 14, wherein said test measurement determines an NBTI (negative bias temperature instability) effect on at least one said target PFET.

17. (Original claim) The method of claim 14, wherein said test measurement is for adjusting a design of MOSFET devices, said method further comprising:

systematically performing at least one stress test on said target PFET; and

taking at least one measurement of each said at least one stress test; and

using said at least one measurement to modify a design parameter of said target PFET.

18. (Original claim) The method of claim 17, wherein said design parameter is used for at least one of correcting a manufacturing process and improving a design characteristic.

19. (Original claim) The method of claim 14, wherein said test is for one of predicting and improving a reliability of one or more MOSFET devices having a structure similar to said target PFET.

20. (Original claim) The method of claim 14, wherein said test is for one of predicting and improving a degradation over time of one or more MOSFET devices similar to said target PFET.